

DOCUMENT-IDENTIFIER: US 3849872 A
TITLE: CONTACTING INTEGRATED CIRCUIT CHIP TERMINAL THROUGH THE WAFER KERF

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ABPL:

A test system for selectively accessing mechanically difficult to access terminals in an integrated circuit chip by the combination of an externally accessible circuit terminal formed in the wafer kerf, a conductive bus bar formed in the kerf connected to the terminal, connecting means for connecting each of a plurality of chip terminals to the conductive bus bar, means for connecting the kerf terminal to a tester, and means for selectively activating a connecting means between the chip terminal and bus bar to provide conductive signal paths from selected chip terminals to the kerf terminal.

CLPW:

at least one externally accessible circuit terminal,

CCXR:

324/158.1

CCXR:

324/765

Draws: Text: Images: HTML: HTML:

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United States Patent

(11) 3,849,872
(43) Nov. 26, 1974

Mubacher

(54) CONTACTING INTEGRATED CIRCUIT CHIP TERMINAL THROUGH THE WAFER KERF

3,849,872 11/872 849,872
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(22) Filed: Oct. 24, 1972

(57) ABSTRACT

(31) Appl. No. 300,678

(52) U.S. Cl. 305/97, 305/98, 307/40, 317/101, 324/151 T

(51) Int. Cl. 305/97, 305/98, 307/40, 317/101, 324/151 T

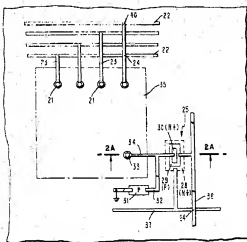
(58) Field of Search 317/235, 22, 221, 101; 307/77, 574, 324/151 T

A test system for selectively accessing mechanically difficult to access terminals in an integrated circuit chip by the combination of an externally accessible circuit terminal formed in the wafer kerf, a conductive bus bar formed in the kerf connected to the terminal, connecting means for connecting each of a plurality of chip terminals to the conductive bus bar, means for connecting the kerf terminal to a tester, and means for selectively activating a connecting means between the chip terminal and bus bar to provide conductive signal paths from selected chip terminals to the kerf terminal.

References Cited

3,849,872 11/872 849,872

8 Claims, 3 Drawing Figures



US-PAT-NO: 6072190
DOCUMENT-IDENTIFIER: US 6072190 A
TITLE: Micro contact pin structure with a piezoelectric element and probe card using the same
----- KWIC -----

Detailed Description Text - DETX (27):
For the semiconductor circuit 7 under test, test signals from a semiconductor test system are provided through the micro contact pins 5 and the resulted output signals are received by the test system. As shown in FIG. 7, such test signals and resulted signals for the corresponding semiconductor circuit are selected by a multiplexing circuit 34 and a multiplexer driver 29 provided on the third silicon substrate 15 of the probe card 3. For example, the multiplexer driver 29 provides a drive signal to the multiplexer circuit 34 to select a group of the micro contact pins 5 corresponding to the semiconductor device 7 under test. Through the multiplexer circuit 34, the selected semiconductor circuit 7 and the semiconductor test system 28 are connected one another via the micro contact pins 5.

G.7

	Document ID	Kind Codes	Source	Issue Date	Pages
30	US 6078537 A		USPAT	20000620	5 Sem
31	US 6072190 A		USPAT	20000608	15 Mic
32	US 5895978 A		USPAT	19990420	8 Hig
33	US 5831993 A		USPAT	19981103	9 Met
34	US 5763882 A		USPAT	19980609	14 Low
35	US 5623420 A		USPAT	19970422	14 Met
36	US 5600148 A		USPAT	19970204	26 Low

Application/Control Number: 09/954,883

Art Unit: 2829

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